Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

**.020”**



**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad: E = .005” X .005”**

**B = .006” X .006”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 1/24/23**

**MFG: FAIRCHILD THICKNESS .009” P/N: BC557**

**DG 10.1.2**

#### Rev B, 7/1